1. A method of forming a silicon-on-insulator device in the fabrication of integrated circuits comprising:

providing a silicon layer overlying an oxide layer on a silicon semiconductor substrate;

etching a first trench into said silicon layer wherein said first trench extends partially through said silicon layer and does not extend to underlying said oxide layer;

filling said first trench with an insulating layer;

etching second trenches into said silicon layer wherein said second trenches extend fully through said silicon layer to underlying said oxide layer and wherein said second trenches separate active areas of said semiconductor substrate and wherein one said first trenches lies within each of said active areas;

filling said second trenches with an insulating layer;

thereafter forming gate electrodes and associated source and drain regions in and on said silicon layer between said second trenches;

depositing an interlevel dielectric layer overlying said gate electrodes;

opening first contacts through said interlevel dielectric layer to underlying said source and drain regions and opening a second contact opening through

said interlevel dielectric layer in each of said active regions wherein said second contact opening contacts both said first trench and one of said second trenches; and

filling said first and second contact openings with a conducting layer to complete formation of said silicon-on-insulator device in said fabrication of integrated circuits.

2. The method according to Claim 1 wherein said first trench is etched into said silicon layer to a depth of between about 1/2 to 3/4 of the thickness of said silicon layer.

3. The method according to Claim 1 wherein said insulating layer comprises a liner oxide layer and a gap-filling oxide layer.

4. The method according to Claim 1 wherein said interlevel dielectric layer comprises one of the group containing sub-atmospheric borophosphosilicate glass (BPSG), tetraethoxysilane (TEOS) oxide, fluorinated silicate glass (FSG), and low dielectric constant dielectric materials and has a thickness of between about 6000 and 20,000 Angstroms.

5. The method according to Claim 1 wherein said conducting layer comprises one of the group containing tungsten and aluminum-copper alloys.

6. The method according to Claim 1 wherein said contact between said first trench and said second trench lowers contact resistance and improves body contact.

7. The method according to Claim 1 wherein said first trench eliminates floating body effects by providing contact to said silicon layer.

8. A method of forming a silicon-on-insulator device in the fabrication of integrated circuits comprising:

providing a silicon layer overlying an oxide layer on a silicon semiconductor substrate;

etching a first trench into said silicon layer wherein said first trench extends partially through said silicon layer and does not extend to underlying said oxide layer and wherein said first trench is etched into said silicon layer to a depth of between 1/2 and 3/4 of the thickness of said silicon layer;

etching second trenches into said silicon layer wherein said second trenches extend fully through said silicon layer to underlying said oxide layer and wherein

said second trenches separate active areas of said semiconductor substrate and wherein one said first trench lies within each of said active areas;

filling said first and second trenches with an insulating layer;

thereafter forming gate electrodes and associated source and drain regions in and on said silicon layer between said second trenches;

depositing an interlevel dielectric layer overlying said gate electrodes;

opening first contacts through said interlevel dielectric layer to underlying said source and drain regions and opening a second contact opening through said interlevel dielectric layer in each of said active regions wherein said second contact opening contacts both said first trench and one of said second trenches; and

filling said first and second contact openings with a conducting layer to complete formation of said silicon-on-insulator device in said fabrication of integrated circuits.

9. The method according to Claim 8 wherein said insulating layer comprises a liner oxide layer and a gap-filling oxide layer.

10. The method according to Claim 8 wherein said interlevel dielectric layer comprises one of the group containing sub-atmospheric borophosphosilicate glass (BPSG), tetraethoxysilane (TEOS) oxide, fluorinated silicate glass (FSG), and low dielectric constant dielectric materials and has a thickness of between about 6000 and 20,000 Angstroms.

11. The method according to Claim 8 wherein said conducting layer comprises one of the group containing tungsten and aluminum-copper alloys.

12. The method according to Claim 8 wherein said contact between said first trench and said second trench lowers contact resistance and improves body contact.

13. The method according to Claim 8 wherein said first trench eliminates floating body effects by providing contact to said silicon layer.

14. A silicon-on-insulator device in an integrated circuit comprising:

a silicon layer overlying an oxide layer on a silicon semiconductor substrate;

shallow trench isolation regions extending fully

through said silicon layer to underlying said oxide layer wherein said shallow trench isolation regions separate active areas of said semiconductor substrate;

a second isolation trench lying within each of said active areas and extending partially through said silicon layer wherein said second isolation trench does not extend to underlying said oxide layer;

gate electrodes and associated source and drain regions lying in and on said silicon layer between said shallow trench isolation regions and covered with an interlevel dielectric layer;

first conducting lines through said interlevel dielectric layer to underlying said source and drain regions; and

a second conducting line within each of said active areas through said interlevel dielectric layer wherein said second conducting line contacts both said second trench and one of said shallow trench isolation regions.

15. The device according to Claim 14 wherein said second trench extends into said silicon layer to a depth of between 1/2 and 3/4 the thickness of said silicon layer.

16. The device according to Claim 14 wherein said shallow trench isolation regions and said second

isolation trench are filled with an insulating layer comprising a liner oxide layer and a gap-filling oxide layer.

17. The device according to Claim 14 wherein said interlevel dielectric layer comprises one of the group containing sub-atmospheric borophosphosilicate glass (BPSG), tetraethoxysilane (TEOS) oxide, fluorinated silicate glass (FSG), and low dielectric constant dielectric materials and has a thickness of between about 6000 and 20,000 Angstroms.

18. The device according to Claim 14 wherein said conducting layer comprises one of the group containing tungsten and aluminum-copper alloys.

19. The device according to Claim 14 wherein said contact between said second trench and said shallow trench isolation region eliminates floating body effects by providing contact to said silicon layer.

20. The device according to Claim 14 wherein said contact between said second trench and said shallow trench isolation region lowers contact resistance and improves body contact.